JUNOS Platforms Training

Juniper™ NETWORKS

Agenda

Introduction

Packet Forwarding Engine

Routing Engine

Packet Flow Example

Summary

Agenda

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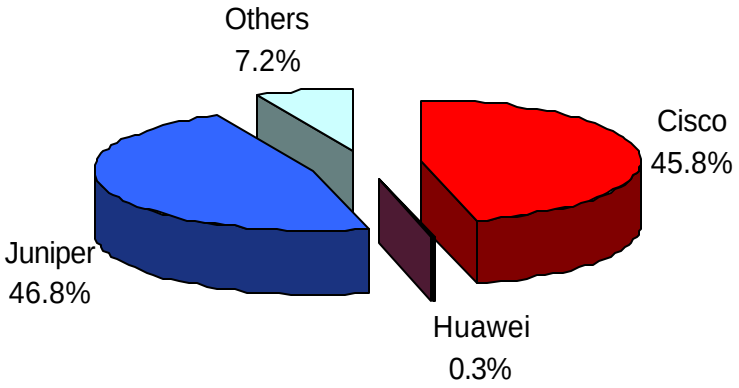
Summary

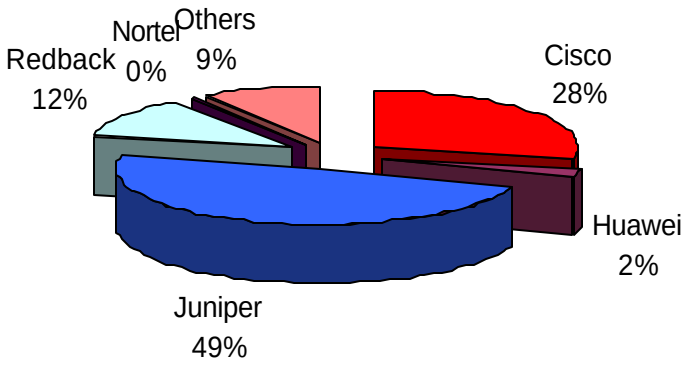
Leadership In Core And BRAS

Core market



#1 in the $73M market!

BRAS market



#1 in the $51M market!

Juniper Networks Portfolio

Secure Meeting

Secure Access SSL VPN

Integrated Firewall/IPSEC VPN

Policy & Service Control

NMC-RX

JUNOScope

Central Policy-based Management

Intrusion Detection and Prevention

BRAS & Circuit

E-series

Remote Edge

J-series

Small/Med Core Circuit Aggregation

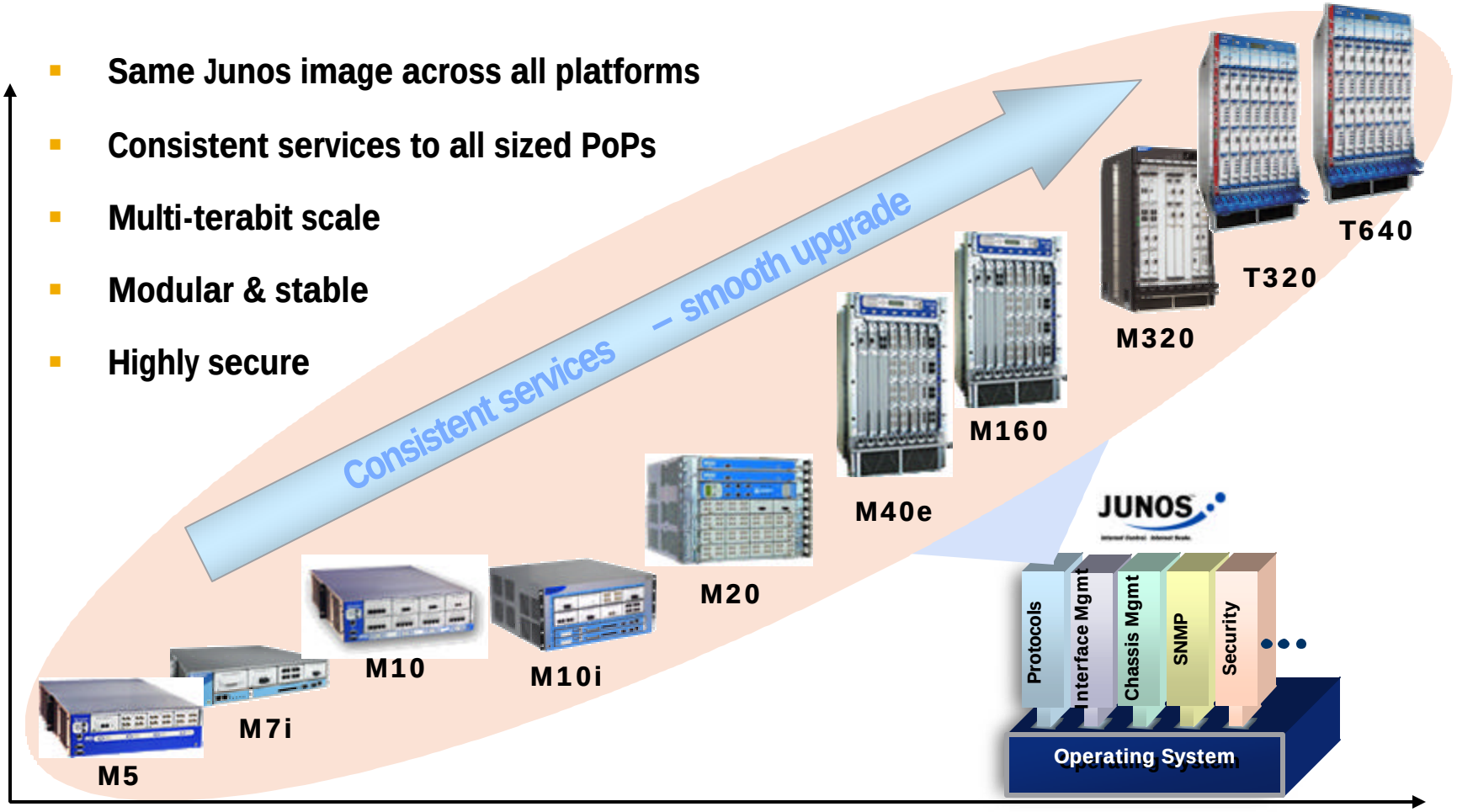
M-series

Large Core Metro Aggregation

T-series

Juniper M-T series product line

- Same Junos image across all platforms
- Consistent services to all sized PoPs
- Multi-terabit scale
- Modular & stable
- Highly secure



M-series – History

- M40 introduced as a core box in 1998
- Introduced edge-focused Internet Processor II in 1999
- Developing edge-features/services for last 5 years
- Introduced IP Services PICs in 2000

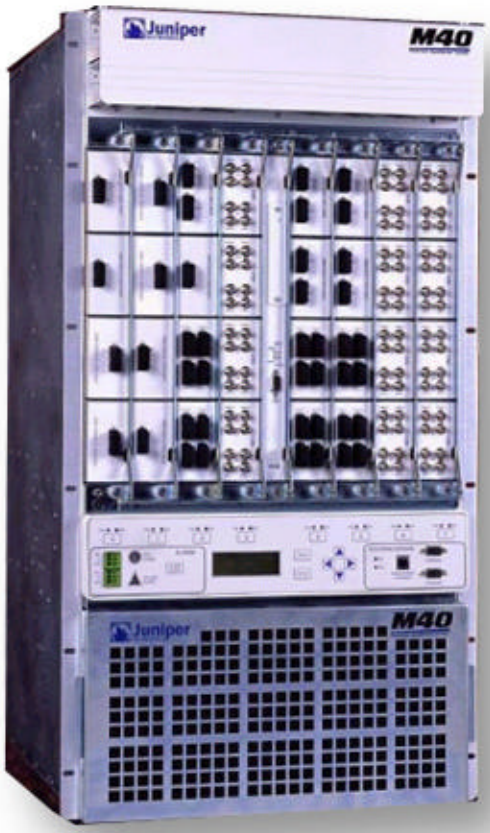
JUNOS Platform History

- FRS history
  - M40→M20 → M160 → M5/M10 →M40e →T640 →T320 →M7i →M10i →M320

- J-series – (CPE) recently announced. It is network-processor based.

M40 Router Overview

- 40 Mpps route look-up engine
- Oversized backplane/ system throughput
- 8 Slots (3+ Gbps/slot)
  - Up to 32 PICs per chassis
- Dual power supplies (AC or DC)
- Two per 7 ft rack
  - 19” (w) x 35” (h) x 23.5” (d)
- JUNOS Internet Software



M20 Router Overview

A space-efficient Internet routing platform for high-speed access, peering, content site, and backbone applications.

- Compact design
  - 14 in (35.56 cm) tall
  - 16 PIC slots, 4 FPCs
- Wire-rate throughput
  - 40 Mpps lookup engine
  - 20 + Gbps throughput capacity
- Fully redundant system
- JUNOS Internet Software

M5 and M10 Overview

Proven performance and reliability in a highly compact form factor for the space- and power-constrained environments of edge markets.

- **Same architecture, ASICs, software, and performance as preceding larger M-series routers**
  - The strength of the core brought to the edge
  - Interface speeds up to OC-48c/STM-16
- **Unparalleled forwarding-engine performance**
  - 40 Mpps lookup engine
  - Aggregate throughput capacity exceeds 12 Gbps
- **Fully redundant system**
- **JUNOS Internet software**
- **Dual power supplies (AC or DC)**
- **Fifteen units per 7’ rack**
  - 19”/48cm (w) x 14”/36cm (h) x 21”/53cm (d)
  - **M5**: 4 PIC slots with 1 built-in FPC
  - **M10**: 8 PIC slots with 2 built-in FPCs

M7i Overview

- Leverages M-series technology
  - Based on M-series Internet Processor
  - Proven JUNOS software
- Four configurations to choose from:
  - 2xFE fixed , 4 open slots, services
  - 2xFE fixed, 4 open slots, no services
  - 1x GE fixed (SFP), 4 open slots, services
  - 1x GE fixed (SFP), 4 open slots, no services
- Uses existing M5/M10 PIC's for investment protection
- Compact at 2 Rack Units high
- Built-in tunnel services
- Redundant Power Supplies

- N x T1/E1
- DS3/E3
- OC3/STM-1
- DS3/E3 ATM
- OC3/STM-1 ATM
- Serial
- N x FE
- GE
- OC12/STM-4

M10i Overview

- Leverages production proven technology
  - Internet Processor II
  - Feature rich JUNOS software
- Uses existing M5/M10 PIC's for investment protection
- Fully redundant configuration available
  - Redundant forwarding engine board
  - Redundant routing engine
  - Redundant cooling
  - Redundant power
  - M20 style redundancy
- Note: No integrated ASM

Ideal for:
Fully redundant PE services solution for lower density PoPs

M320 Overview

- Most scalable control
  - New 1Gbps RE to PFE link for increased logical and channelized interfaces plane
  - New RE1600 for increases in BGP sessions, routes, VRFs
  - Service rich & highly stabled JUNOS, scaled in production
- Most scalable forwarding plane
  - 10Gbps uplinks, 320 Gbps throughput
  - 385 Mpps lookup
- Optimized for QoS/Multi-Service
  - 8 queues per interface
  - Per DS0, VC, VP, DLCI, VLAN QoS
- Investment protection
  - PIC portability from M40e/M160/T-series
  - Backplane designed to accept future FPC upgrades
- Collocation Friendly Design
  - Chassis Depth-reduction: Fits in 800 mm cabinets
  - AC and DC PEMs sized to less than 60AMPs feeds

T640 Overview

- First platform optimized for 10Gbps
  - Density
  - Performance
  - Scale
  - Serviceability
  - Reliability
- Smooth Upgrade path to 40Gbps
  - OC768c/STM-256 “ready”
- 4 Times Performance of M160 in same space
  - 32 x OC-192c/STM-64/10 GigE
  - 640 Gbps chassis capacity
  - 770Mpps
- No single point of failure

T320 Overview

- T320 router: High density 10GE/10G POS aggregation/core router
  - Compact 1/3 rack form factor
  - Less power: 60 A @ -48 V; 2,880 W
  - Lower-speed interfaces (OC-3/STM-1, OC-12/STM-4 ATM and SONET/SDH, GE, FE)
- Scales to dense 10 Gbps
  - 16 x OC-192c/STM-64 or 10-Gbps Gigabit Ethernet per 1/3 rack
  - 64 x OC-48c/STM-16 per 1/3 rack
  - 320-Gbps throughput; 385-Mpps forwarding

Introducing J-series Services Router
Carrier-class Routing with Superior TCO

J2300

- Up to 4 Mbps uplink capacity
- 2 fixed FE LAN + 1 WAN + 1 expansion slot

J4300

- Up to 16 Mbps uplink
- 2 fixed FE LAN + 6 open WAN slots

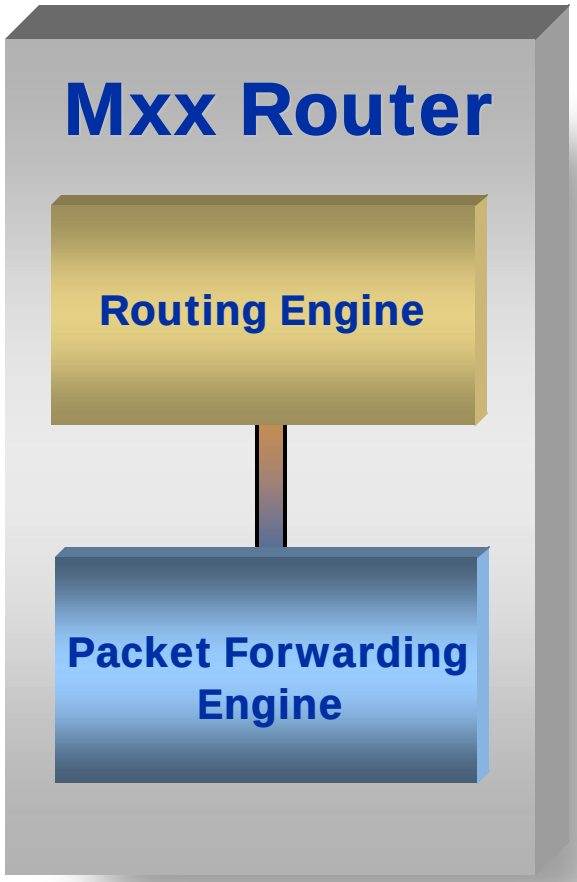
J6300

- Up to 90 Mbps uplink
- 2 fixed FE LAN + 6 open WAN slots
- Redundant power supply

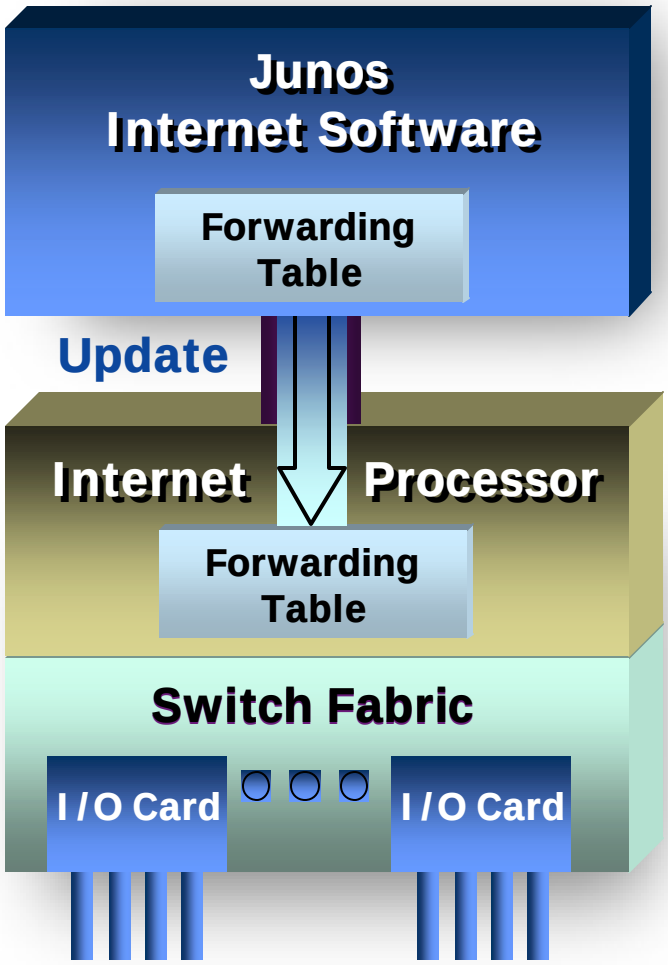
- Higher uptime through secure, reliable software delivers business critical traffic
- Superior performance through modern OS + per I/O processors provides high throughput w/ features
- Lower OPEX with management features optimized for remote sites
- Lower CAPEX with licensing flexibility to scale investment w/ requirements
- Value add features for the service provider/managed service channel

System Architecture

- Routing Engine (RE)
  - Intel-based
  - JUNOS Internet Software
- Packet Forwarding Engine (PFE)
  - ASIC-based design
  - FPCs and PICs
- Clean separation of routing and packet forwarding functions
  - Consistent performance
  - Stability
  - Carrier grade



System Architecture



Routing Engine

- Uses knowledge of network to construct a packet forwarding table

Packet Forwarding Engine

- Copies packets from an input interface to an output interface based on the packet forwarding table

Agenda

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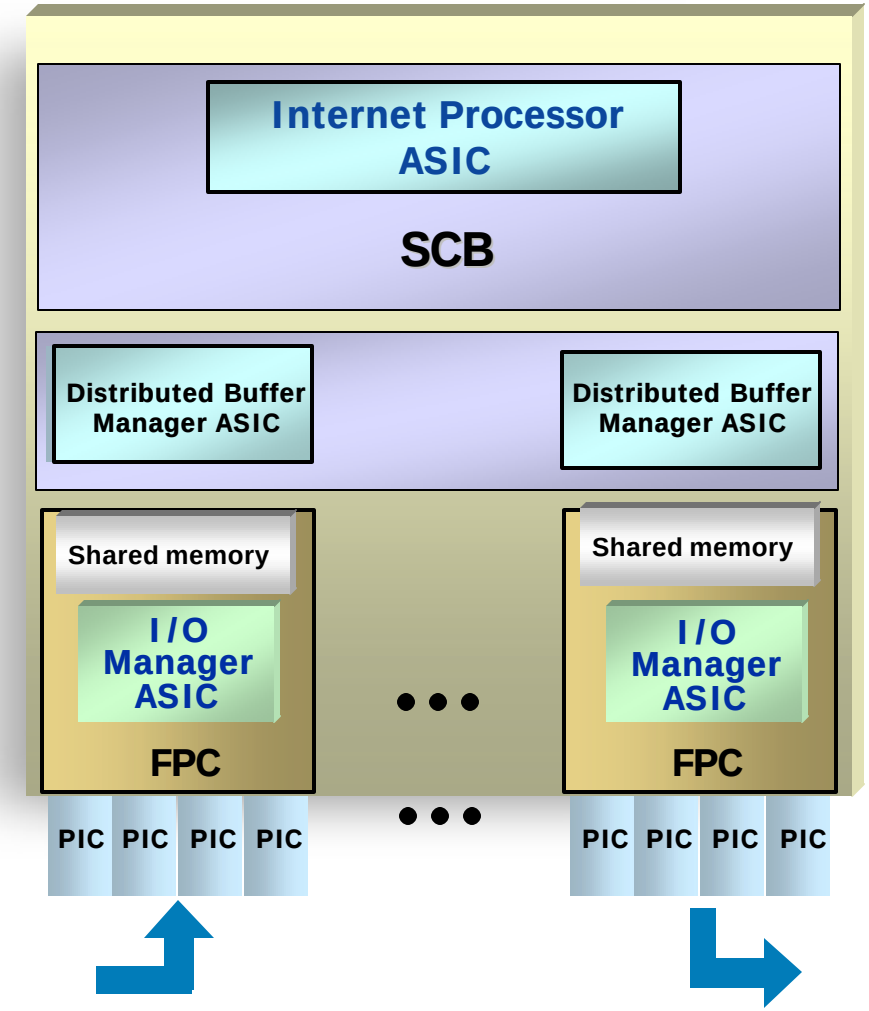
Summary

PFE Overview

- FPCs
  - Hardware platform which accepts PICs
- PICs
  - Physical Interface Card
  - Contains physical layer components
- Control board with internet Processor ASIC
  - FEB M5/M10
  - SSB M20
  - SCB M40
  - SFM M160/M40e

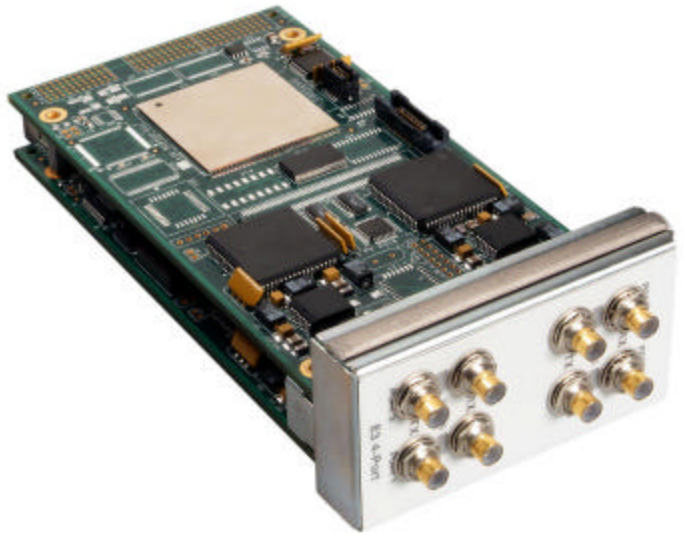
M-series PFE Architecture

- Simplicity
  - One forwarding table
  - One lookup
  - Single-stage, shared memory
    - One packet write
    - One packet read
- 40 Mpps performance
- Highly integrated for minimal space and power
- Wire Rate Forwarding
  - Unicast
  - Multicast
  - Class-of-service queuing



T3 and E3 PICs

- 4 ports per PIC
- Wire-rate throughput
- Integrated DSU
- Large MTU (up to 9192 bytes)
- Scrambling support
- ITU G.751 Framing
- Interoperability
  - Digital Link
  - Kentrox
  - Larscom

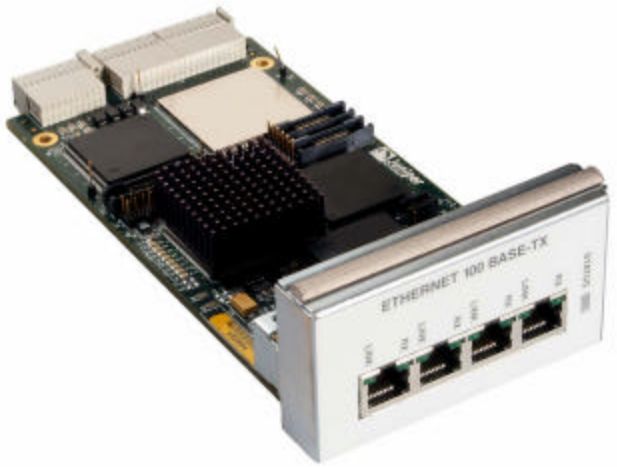


Gigabit Ethernet PIC

- Line-rate performance for all packet s
  - 64 through 9192 bytes
- Source MAC address filtering
- Autonegotiation between link partner
- SX and LX optics
- Full-duplex operation
- VRRP and 802.1Q VLAN support

Fast Ethernet PIC

- 4 ports per PIC
- Wire-rate
- Auto-sensing full and half-duplex modes
- Large MTUs, up to 4,470 bytes
- VRRP and 802.1Q VLAN support
- MAC address filtering
- MAC Address Accounting for 128 sources
- Two-pair, category 5 unshielded twisted pair connectivity through 100Base-TX RJ-45 connector

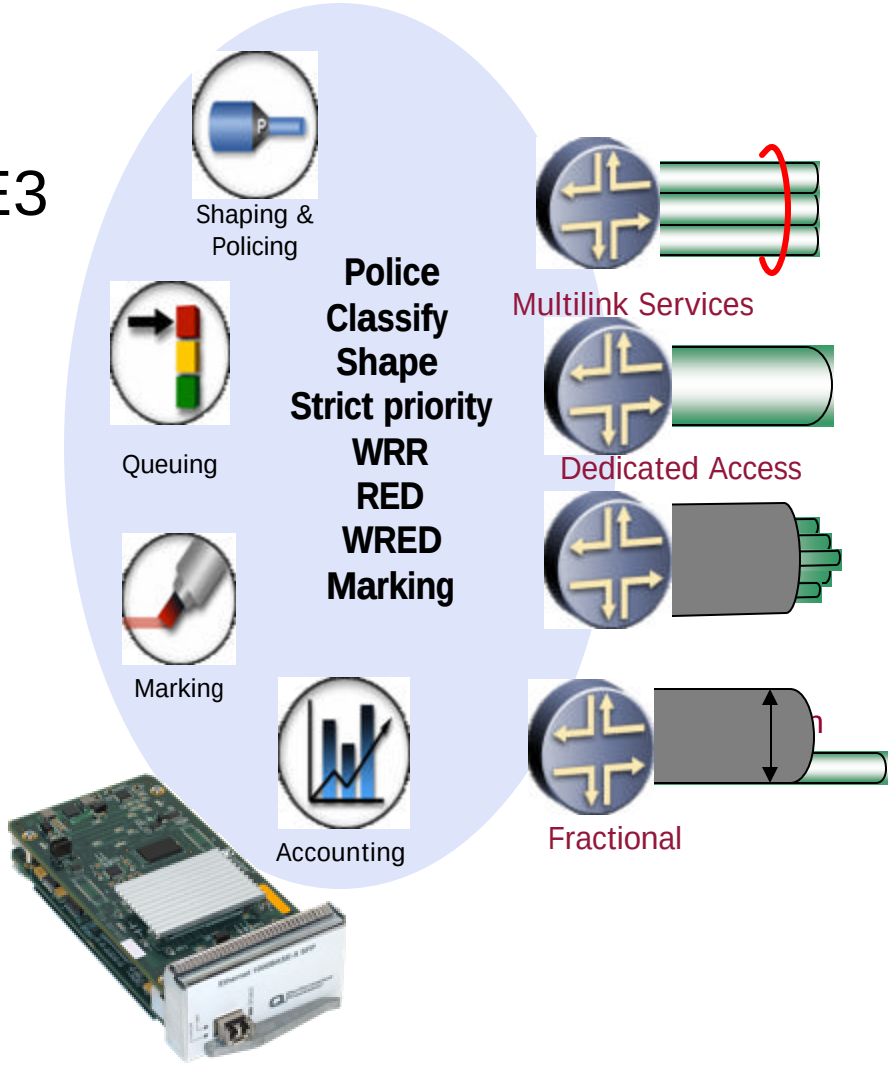


SONET/SDH PICs

- OC-192c/STM-64
  - M160 only, uses all 4 PIC slots
- OC-48/OC-48c/STM-16
  - M20 and M40—1 port per FPC, use
  - M160—1 port per PIC, 4 per FPC
- OC-12/OC-12c/STM-4
  - 1 port per PIC, 4 per FPC
- Channelized OC-12
  - 1 port per PIC, 4 per FPC
- OC-3c/STM-1
  - 4 ports per PIC, 16 per FPC

Edge-optimized PICs

- IQ PICs (Intelligent Queuing)
  - ATM2, Channelized, GE, E3
  - Granular per-logical interface QoS



Overview

Performance Processor

- QPP - Foundation for family of Edge interfaces
  - ASIC purpose-built for service provider edge deployments
  - It's now named IQ PIC family
- Design Philosophy:
  - Enable revenue generating services per customer through advanced QoS
  - Reduce operating inefficiencies through increased customer density, scale and operational simplicity
- Juniper's second generation of dedicated access interfaces
  - Leverage learnings from existing edge interface already deployed in production environments
- Enhance functionality of JUONS routers at the edge
  - Stability of a core router architecture merged with service creation

IQ PIC Family

Category	Q1 2003	Q2 2003	Q3 2003	Q4 2003/2004
T1/E1 Aggregation	◆ 10xCHE1QPP ◆ 4xCHDS3QPP	◆ 1xCHSTM1QPP		
DS3/E3 Aggregation	◆ 1xCHOC12QPP			
Higher-speed Aggregation	◆ 1xCHOC12QPP			
Ethernet Aggregation		◆ 2xGEQPP-SFP	◆ 1xGEQPP-SFP	

** Note: All Q-PICs are only supported on Enhanced FPCs.

Gigabit Ethernet IQ PIC

- Based on Q chip Performance Processor (QPP)
- Small Form Factor Pluggable (SFP) optics
- Four queues for class of service
  - **Per VLAN, WRR or strict priority Scheduler**
  - **RED and Weighted RED**
  - **Ingress and Egress Policing**
  - **Egress Shaping**
- **8 queues for Gimlet platforms**
- **4 queues for Martini platforms**
- Applications:
  - **Metro Ethernet**
  - **Dedicated access**

Gig E QPP based PIC
1-port, 767 VLANs/port 2-port, 383 VLANs/port
4/8 queues per VLAN
SX,LX and LH optics types
VLAN ID field re-write operations
VLAN and MAC address filtering and accounting

ATM IQ PIC

- Special IQ PIC - Not base on QPP chip (still name it “IQ”)
- ATM2 OC-3 and OC-12 PICs
  - Next generation ATM PIC that provides greater traffic visibility and control by enhancements to:
    - VP/VC shaping
    - VPI/VCI range
    - Cell relay performance
    - Diagnostics
  - Single-mode or Multi-mode optical interface type
  - Six (6) models of the PIC:
    - ATM2 2-port OC-3 SM/MM FPC1 for M160 and Bombay
    - ATM2 1-port OC-12 SM/MM FPC1 for M160
    - ATM2 2-port OC-12 SM/MM FPC2 for M160 & T-

1-port OC-12/STM-4 ATM IQ PIC, single-mode

2-port OC-3/STM-1 ATM IQ PIC, single-mode

Tunnel PIC

- Supports
  - Generic route encapsulation (GRE)
  - IP-IP
- Useful for multicast support
  - Transports PIM sparse mode packets through network cloud to rendezvous point (RP)
- Provides line-rate encapsulation and decapsulation of packets up to OC-12 (M40/M20) or OC-48 (M160) speeds

Encryption Services PIC

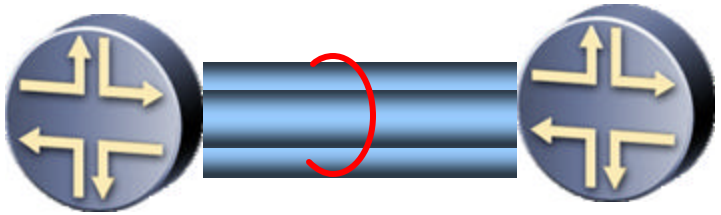
- IPSEC features
  - ESP Tunnel Mode for encrypting data traffic
  - HMAC-MD5 and HMAC-SHA1 authentication
  - DES-CBC and 3DES-CBC encryption
  - Pre-shared manual keys
- IKE features
  - Automated key management
  - Main IKE mode supported for IKE SA setup
  - Quick mode supported for IPSec SA setup
- Scalability
  - 800Mbps (half-duplex) of encrypted throughput per PIC
  - 1000 tunnels per PIC (2000 SA's)

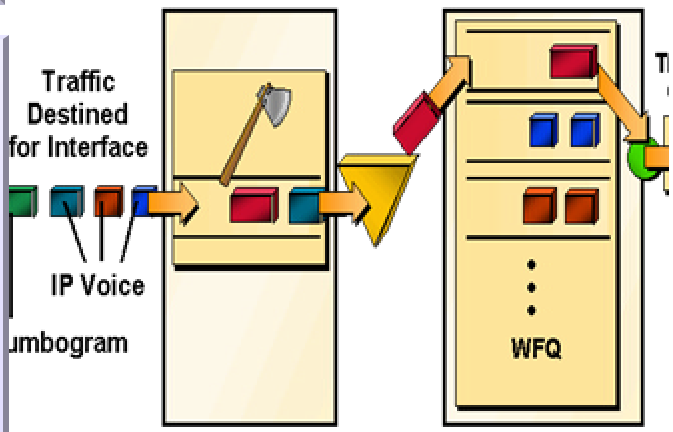
Link Services – ML/LFI

- Multilink Services via interworking with ML and LS PIC
- Significant pricing differential between T1 to DS3 and E1 to E3
- Leverages widely deployed T1/E1 copper circuits
- Certain regions have no availability of DS3/E3 circuits
- Reduce customer churn for smaller SPs

- VoIP services via interworking with LS PIC's Link Fragmentation and Interleaving
- LFI reduces delay and jitter for real-time applications on low-speed links
- LFI Essential for voice and data over same link
- Required to meet SLAs for voice traffic

Highly Flexible, Highly Scalable MLPPP Bundle





Passive Monitoring PIC

- Security and traffic analysis services
- Available for M40e and M160 routers
  - Router used in a nonforwarding “passive mode”
  - PM PIC requires external optical splitter
- Monitors IPv4 packets and flows over SONET/SDH on
  - OC-3c/STM-1, OC-12c/STM-4, and OC-48c/STM-16
  - PPP or HDLC (Cisco) layer 2 encapsulations
- Generates cflowd v5 records for export to collector nodes
  - IPSec or GRE tunnels can be used for exporting
- Uses firewall filters to select traffic types
- Performance - 100K pps at 400 bytes

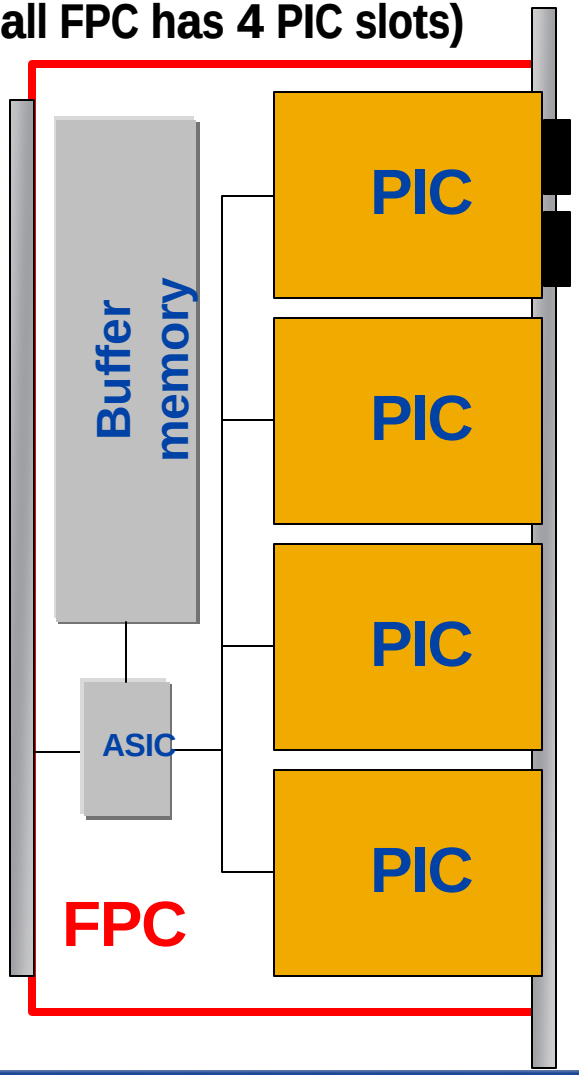
Adaptive Services PIC

- Offers multiple services integrated on a single PIC
- Enables new, integrated service offerings
- Hardware enabled, high performance
- Services:
  - **NAT functions**
  - **Stateful Firewall**
  - **DoS prevention**
  - **Attack Detection**
  - **Tunneling services**

Adaptive Services PIC
500 Mbps per PIC
400K unidirectional sessions
12K sessions/second setup

FPC/PIC

FPC - A holder of PICs (not all FPC has 4 PIC slots)



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Routing Engine

Packet Flow Example

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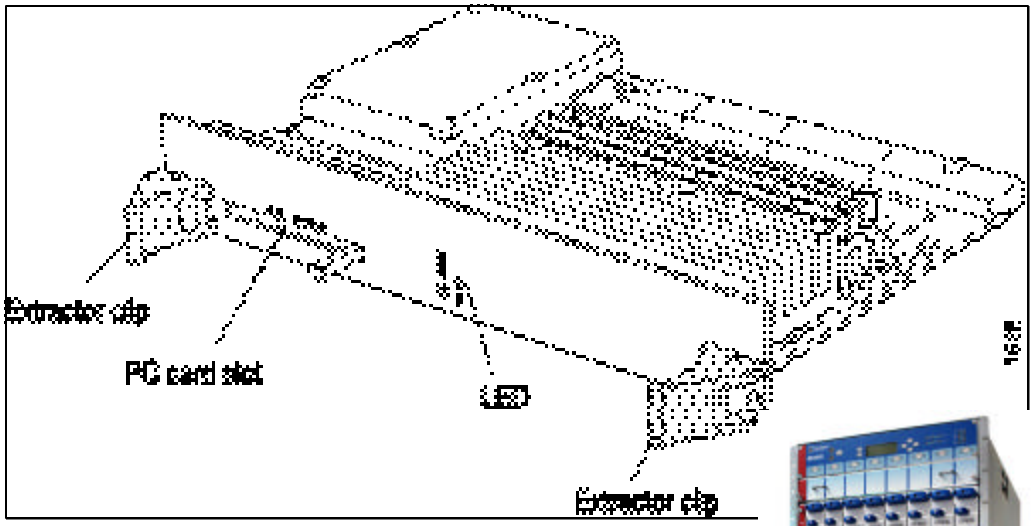
Routing Engine Overview

- JUNOS software resides in flash memory
  - Alternate copy available on hard drive
- Provides routing protocol intelligence to PFE
  - Not directly involved with packet forwarding
- Implements command-line user interface
  - Operations
  - Administration
  - Maintenance
  - Provisioning
- Manages care and feeding of PFE

RE-600-2048-BB

- New Routing Engine (RE3)
- 600MHz Pentium III
- 2GB ECC RAM
- 96MB Flash
  - Primary storage
- 30GB HDD
  - Secondary storage
- PC-Card slot
- Can be used in M5/M10/M20/M40e/M160/T320/T640



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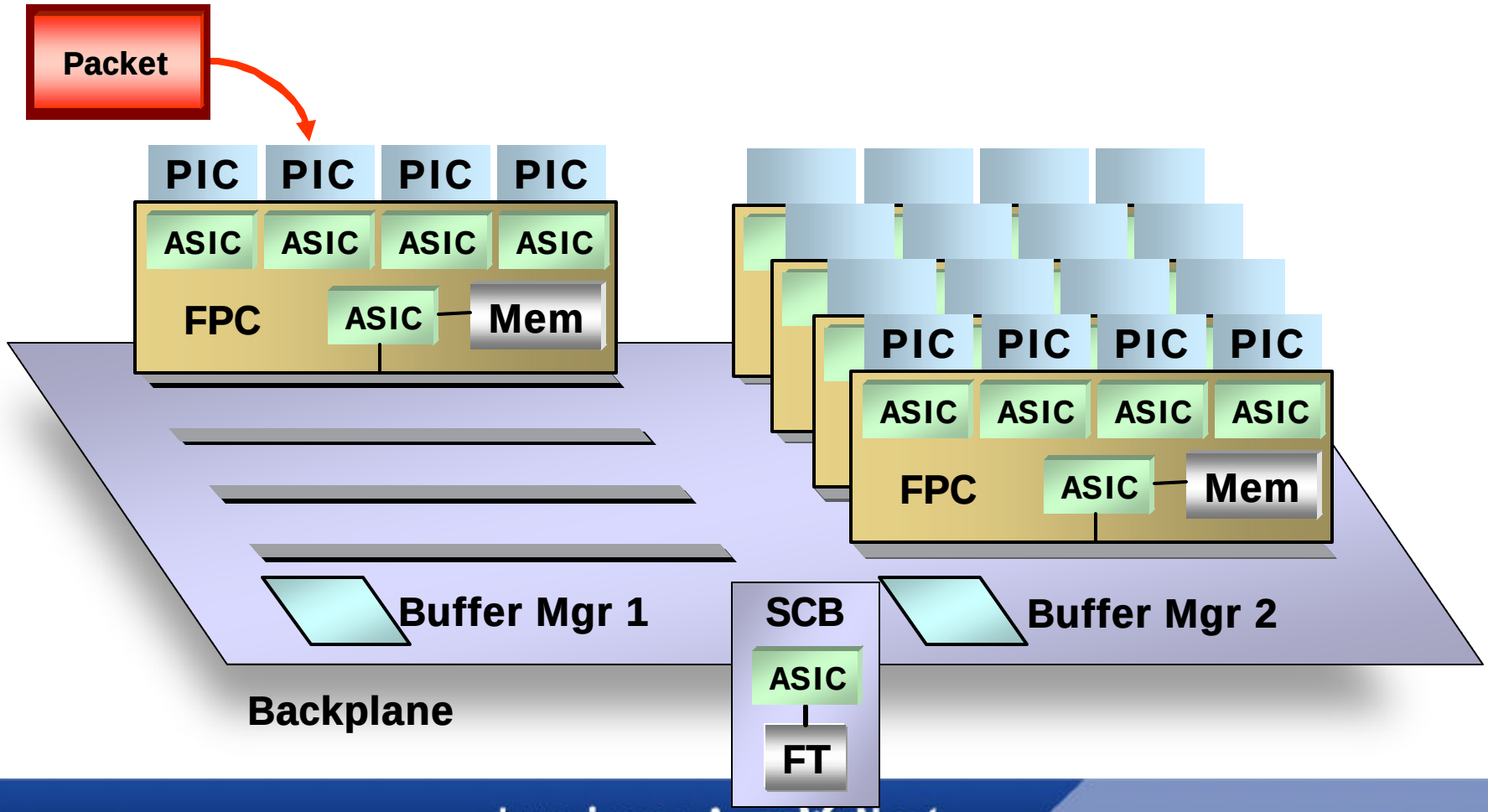
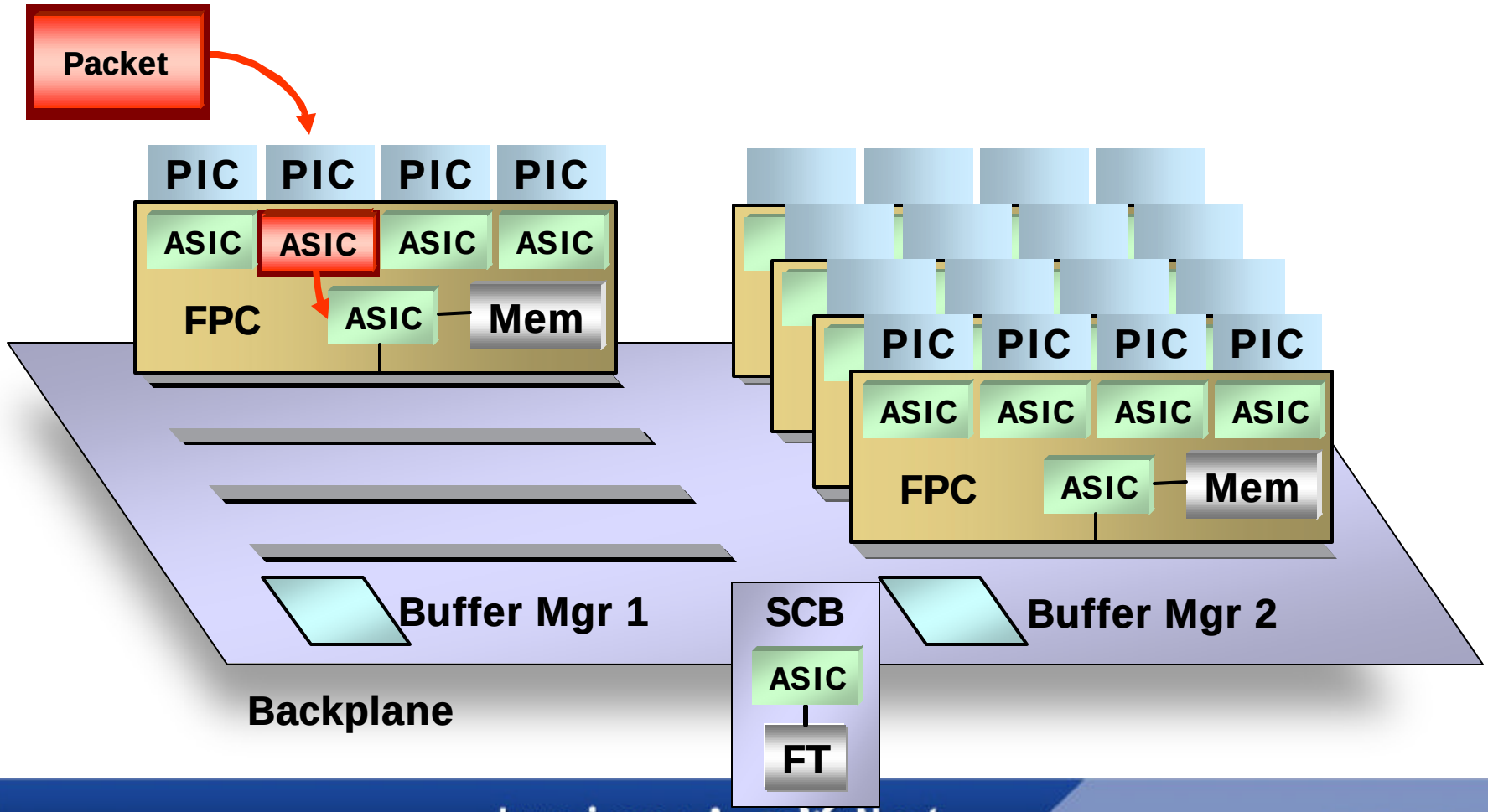
Packet Flow Example

- Packet arrives at PIC on fiber optic cable



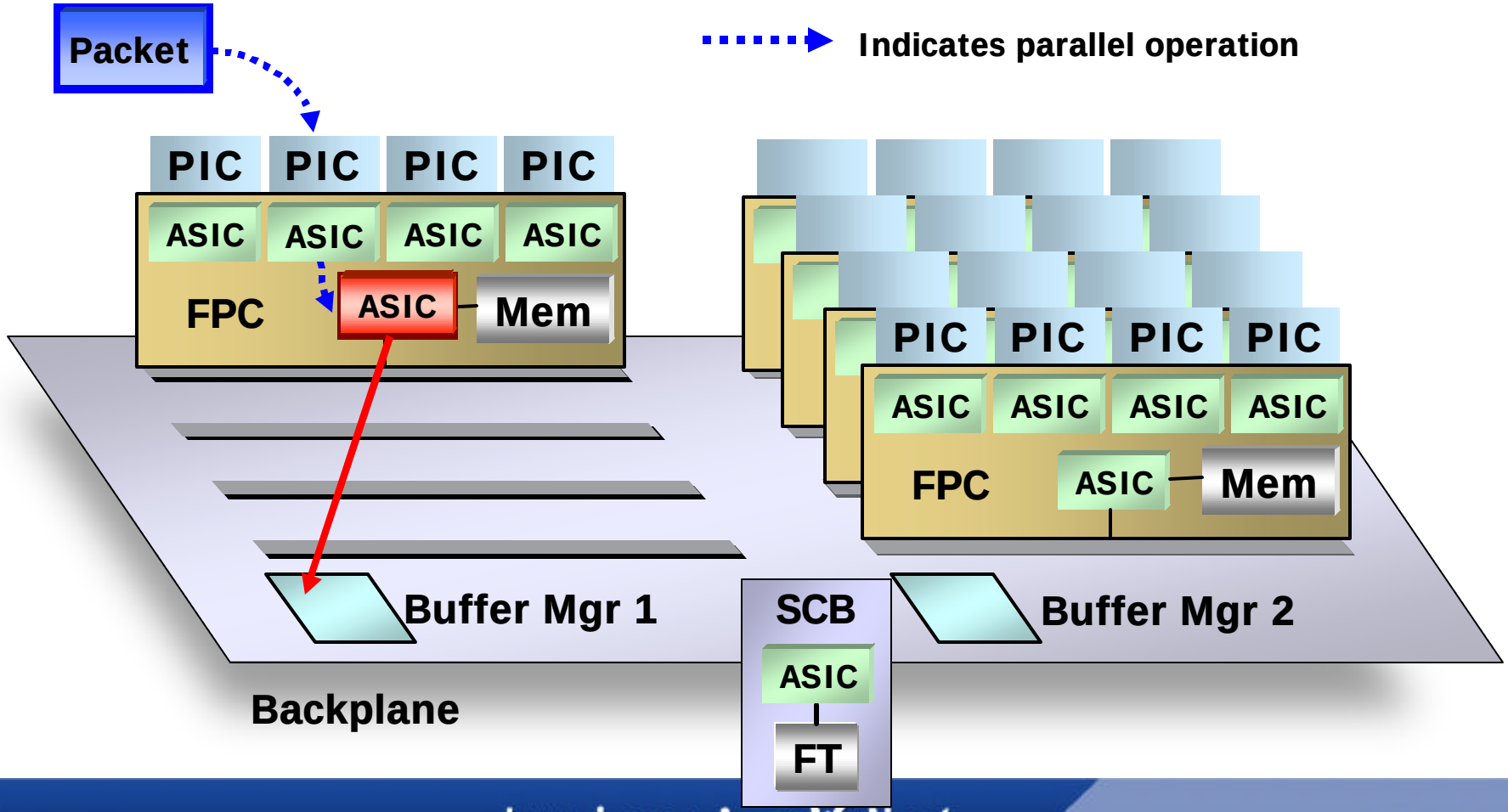
Packet Flow Example

- PIC ASIC extracts data, gives to FPC ASIC



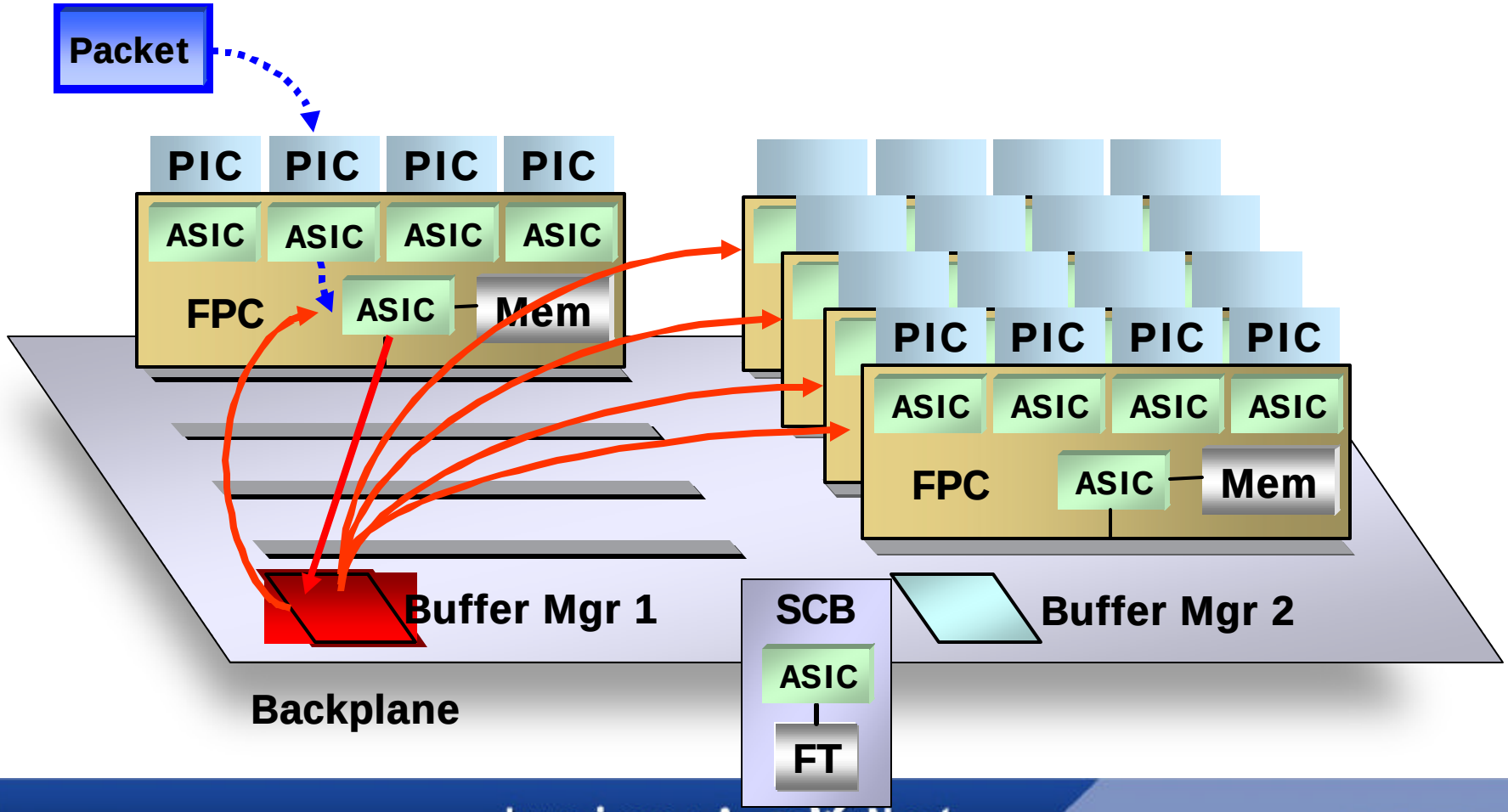
Packet Flow Example

- FPC ASIC chops up data, feeds to Buffer Mgr 1



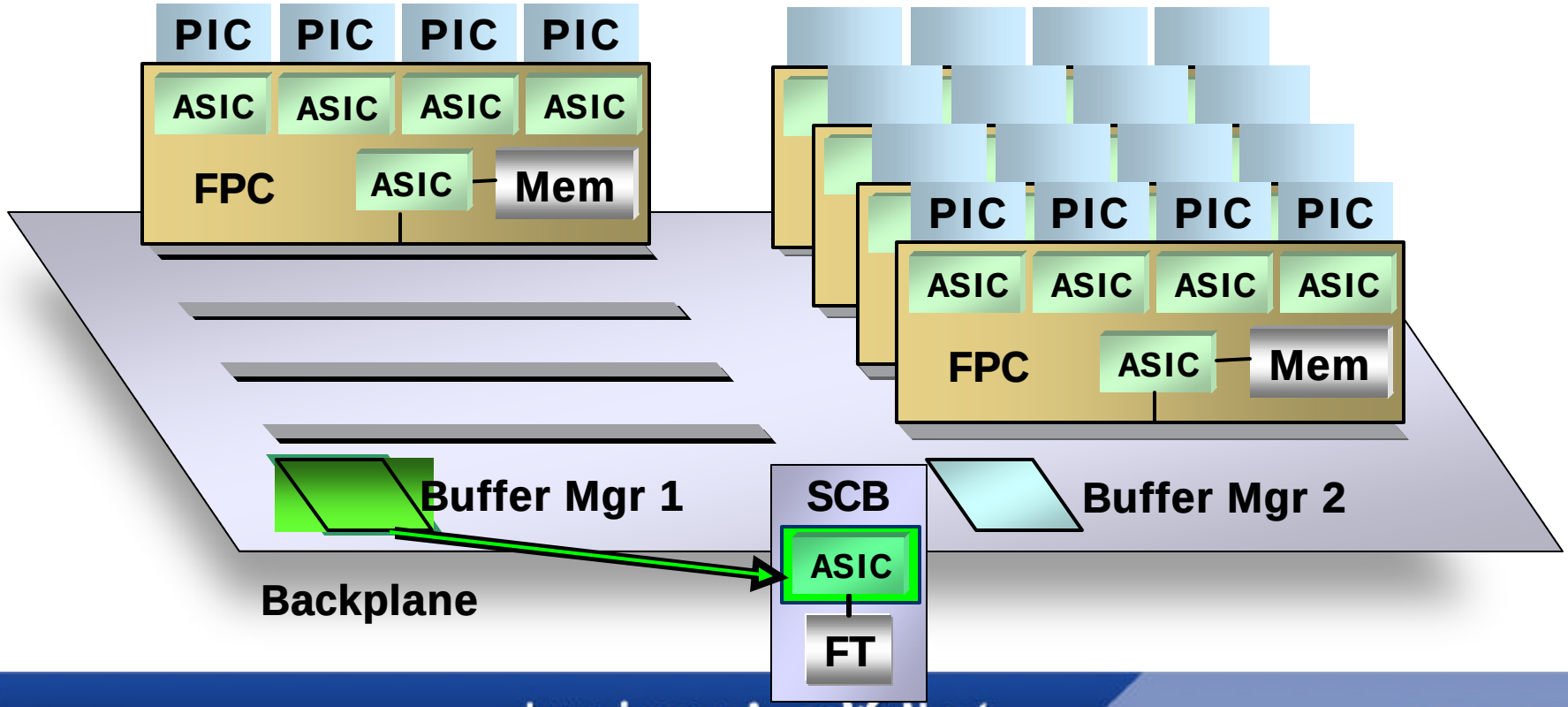
Packet Flow Example

- Buffer Mgr 1 sprays J-cells to shared FPC memory



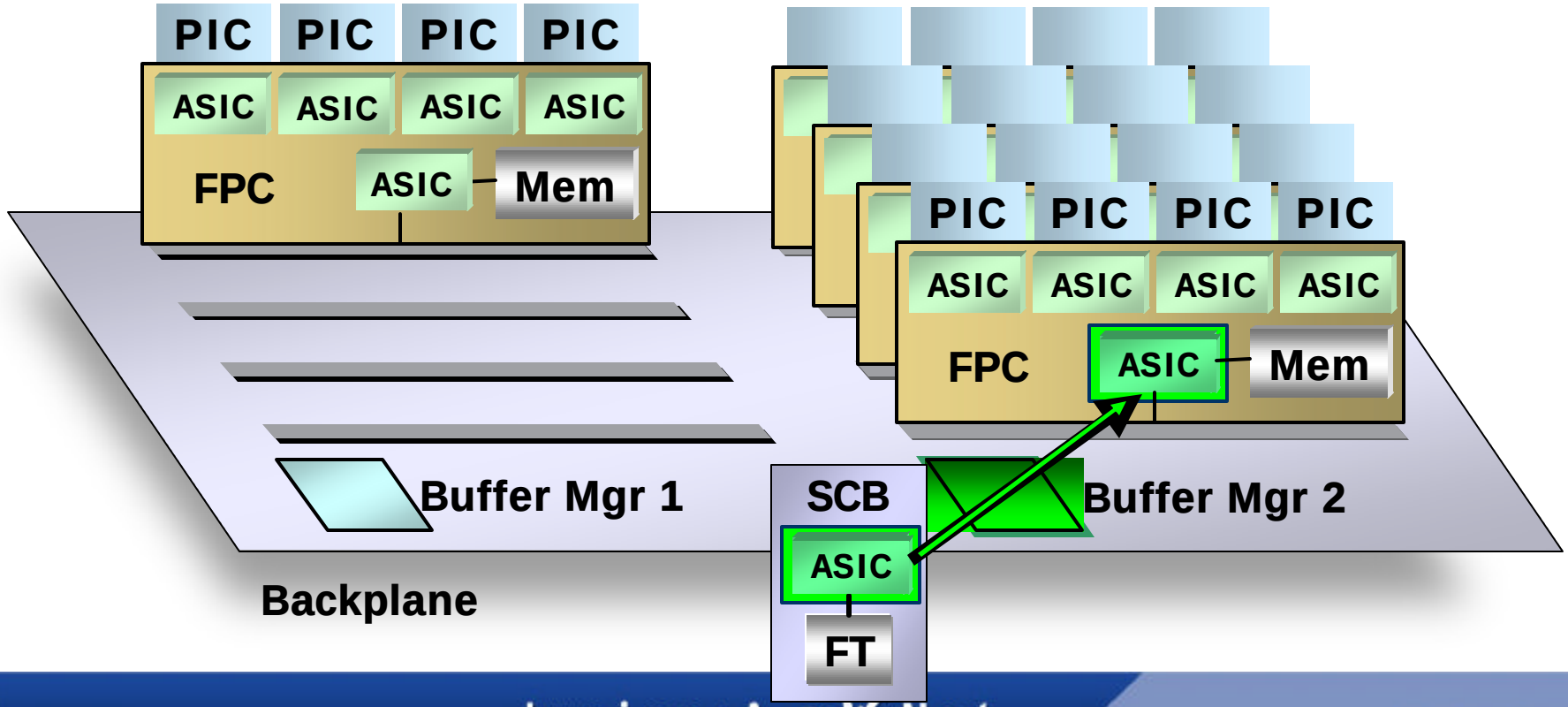
Packet Flow Example

- Buffer Mgr 1 tells Internet Processor destination address and locations of stored J-cells



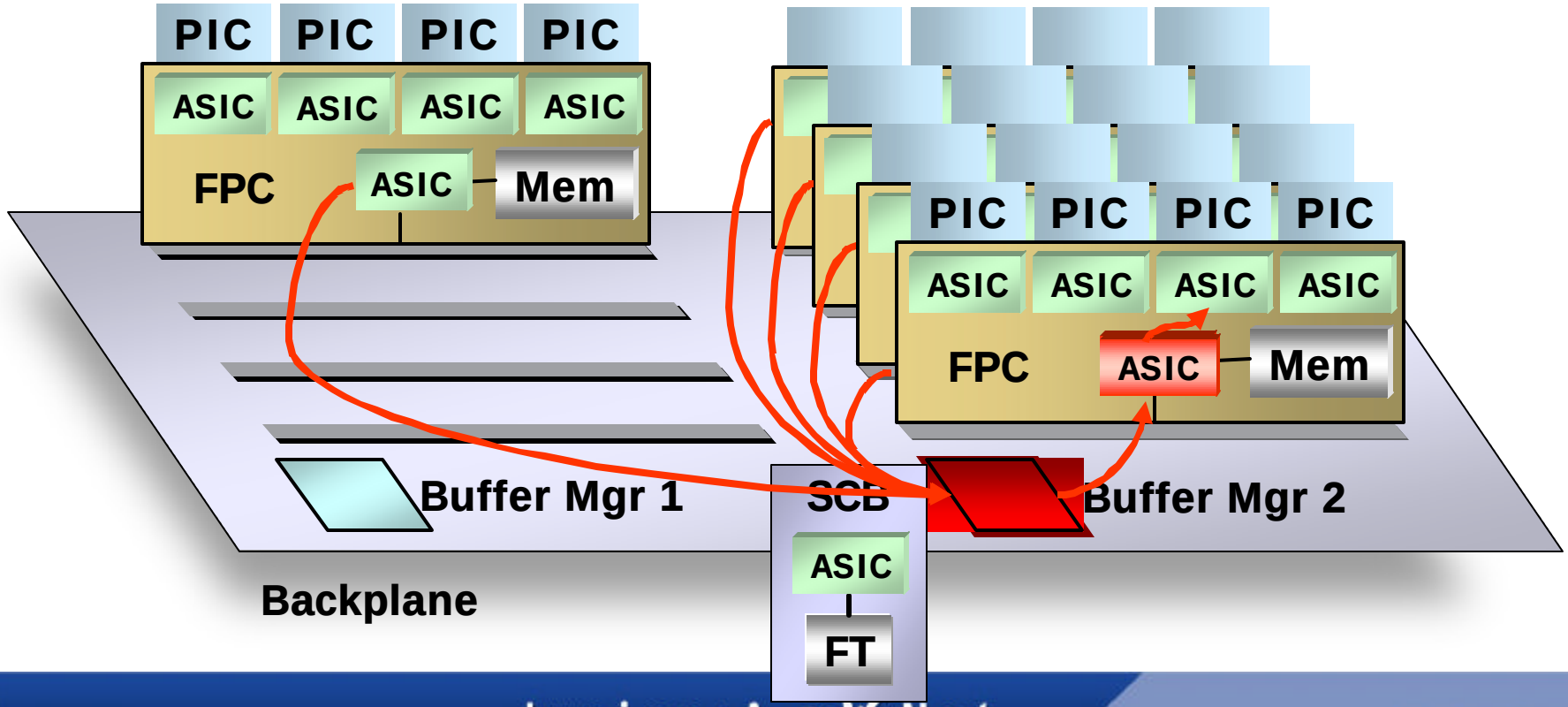
Packet Flow Example

- Internet Processor looks up destination FPC and notifies Buffer Mgr 2, which passes notification to destination FPC(s).



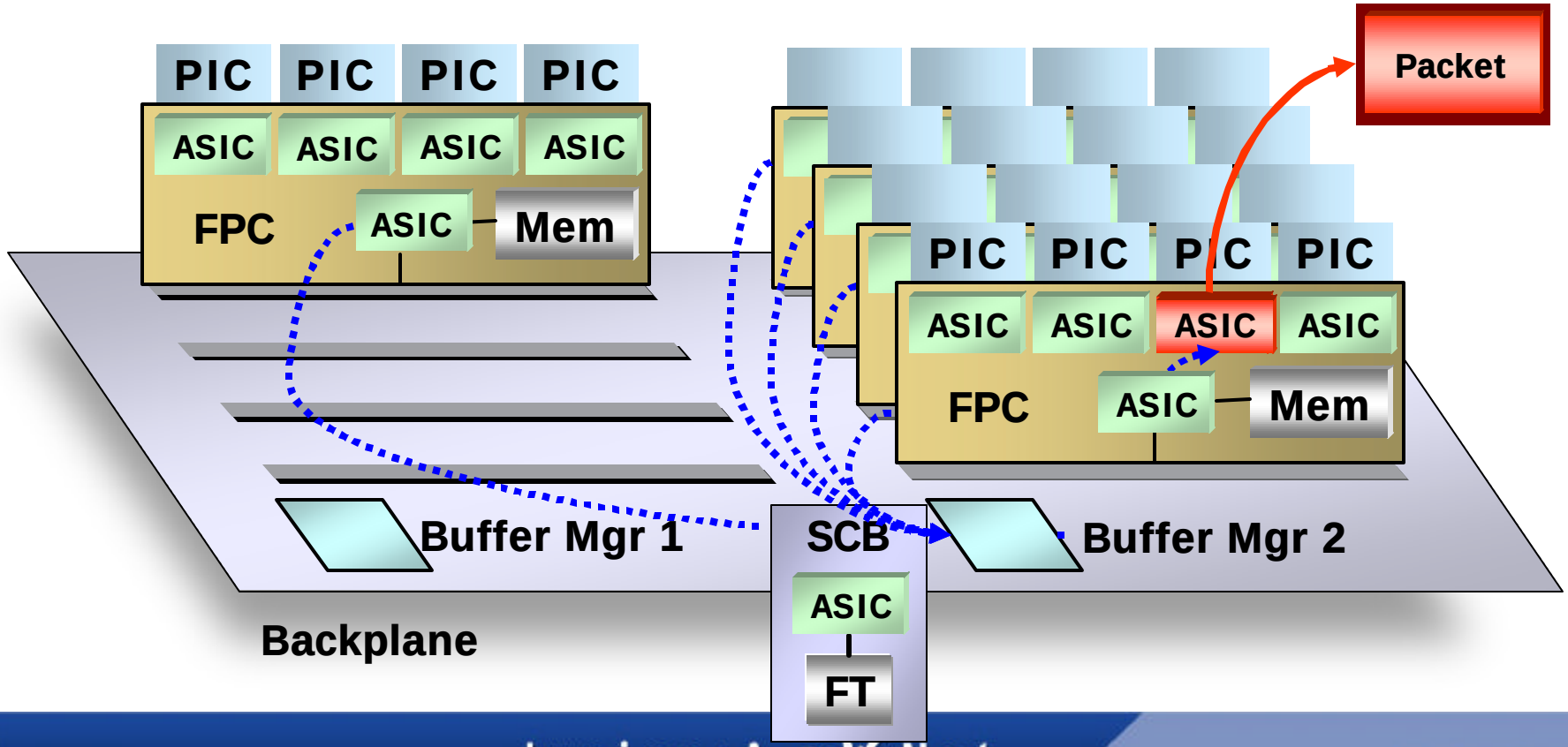
Packet Flow Example

- FPC ASIC performs queuing and CoS then requests J-cells from shared memory and adds appropriate link encapsulation on way to PIC



Packet Flow Example

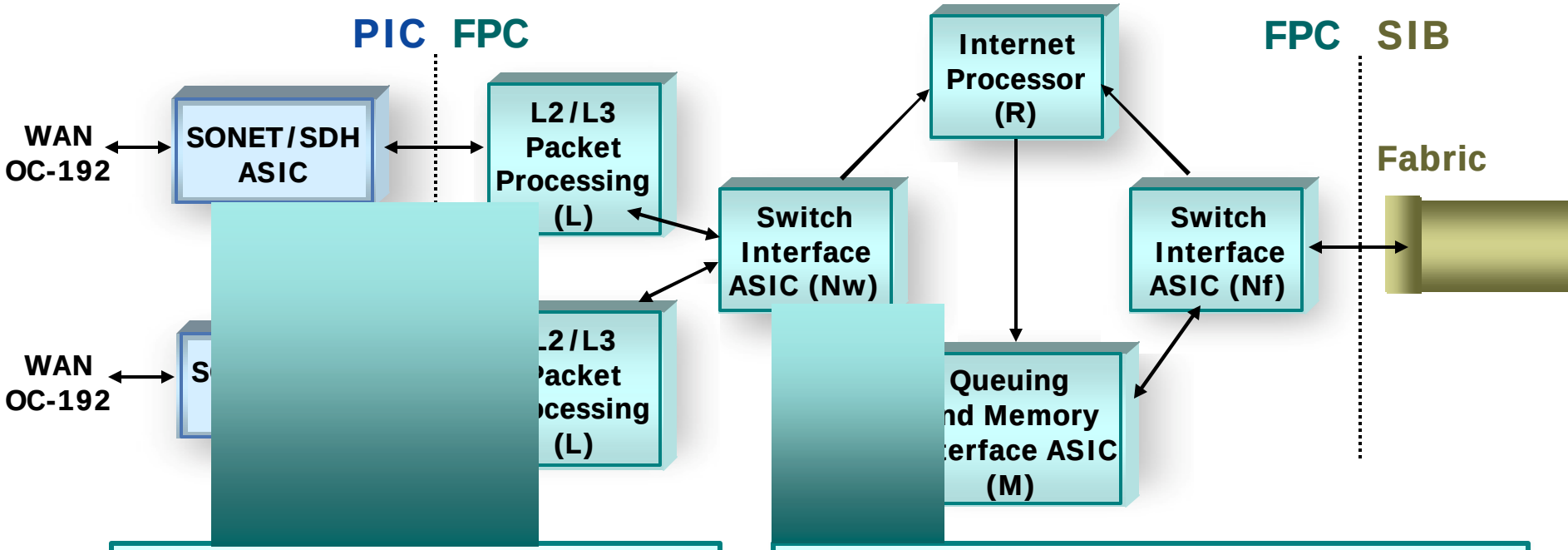
- PIC ASIC adds physical layer framing, CRC and sends bit stream out to the “wire”



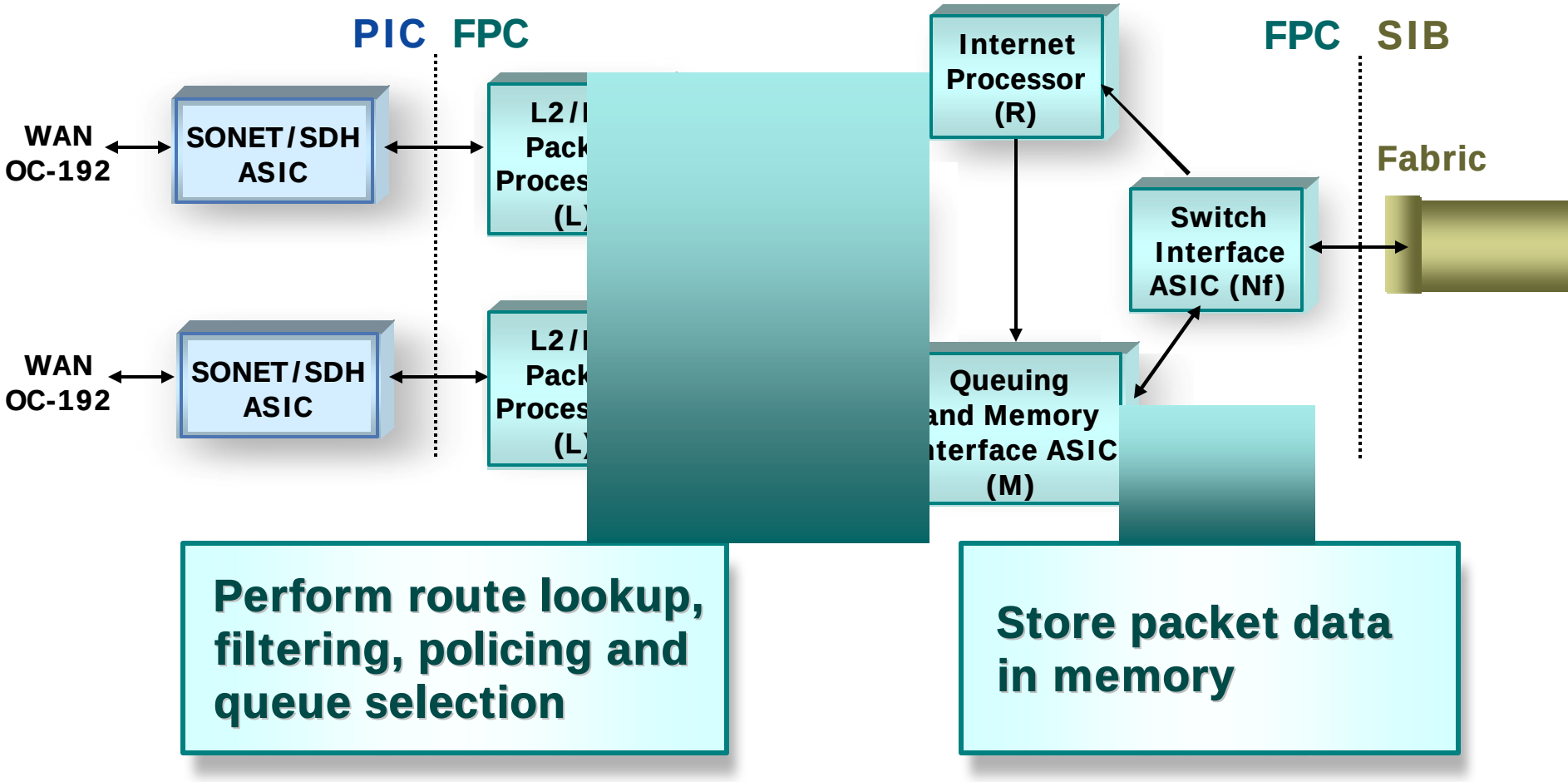
Advantages of Distributed Architecture

- Building a scalable, fault-tolerant switch is easier than a scalable, fault-tolerant shared memory
- Hardware and software failures are localized
- Software architecture can be distributed
  - Route lookups can be split over ingress and egress chassis
  - Multichassis system can be configured as multiple independent routers interconnected by the switch fabric

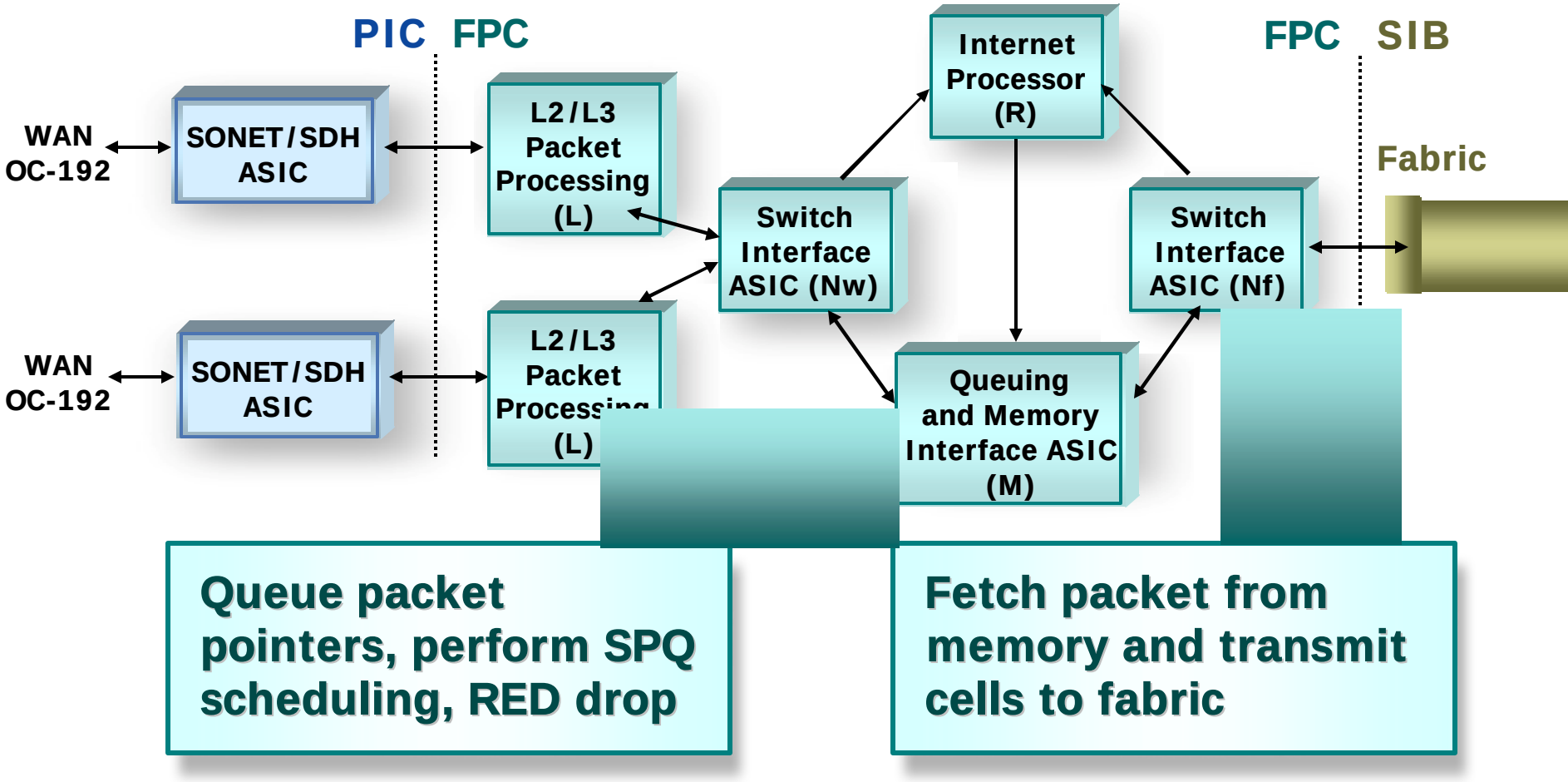
Ingress Packet Flow



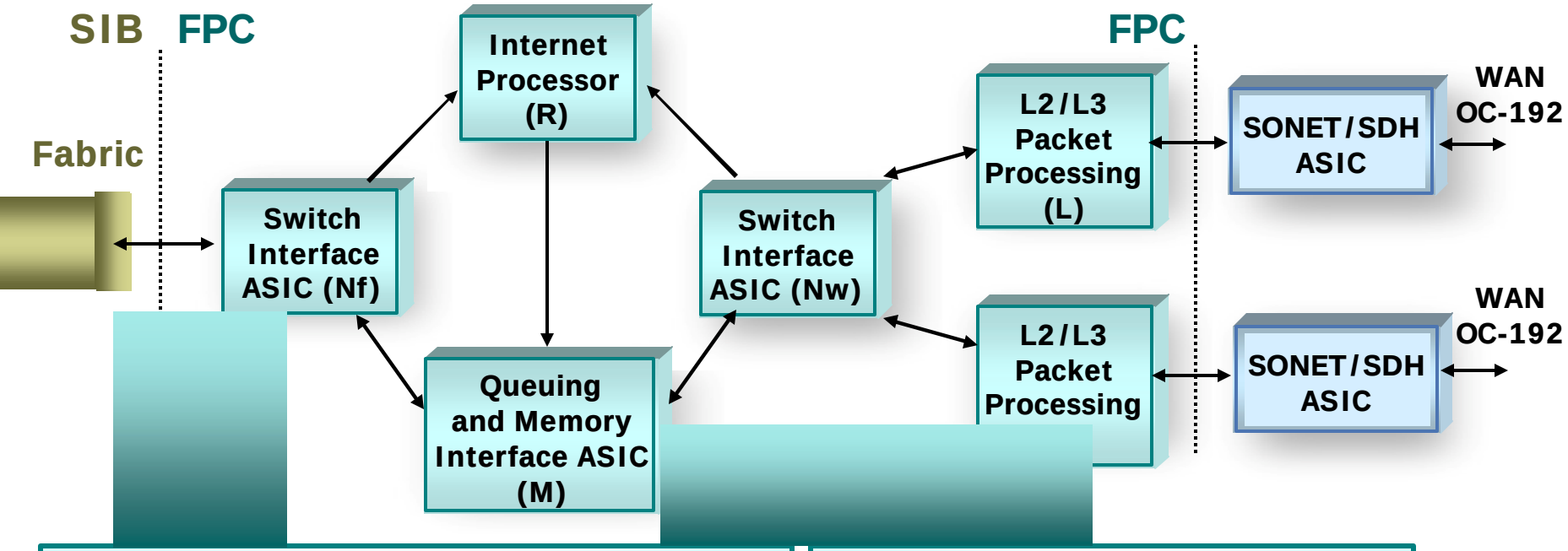
Ingress Packet Flow



Ingress Packet Flow



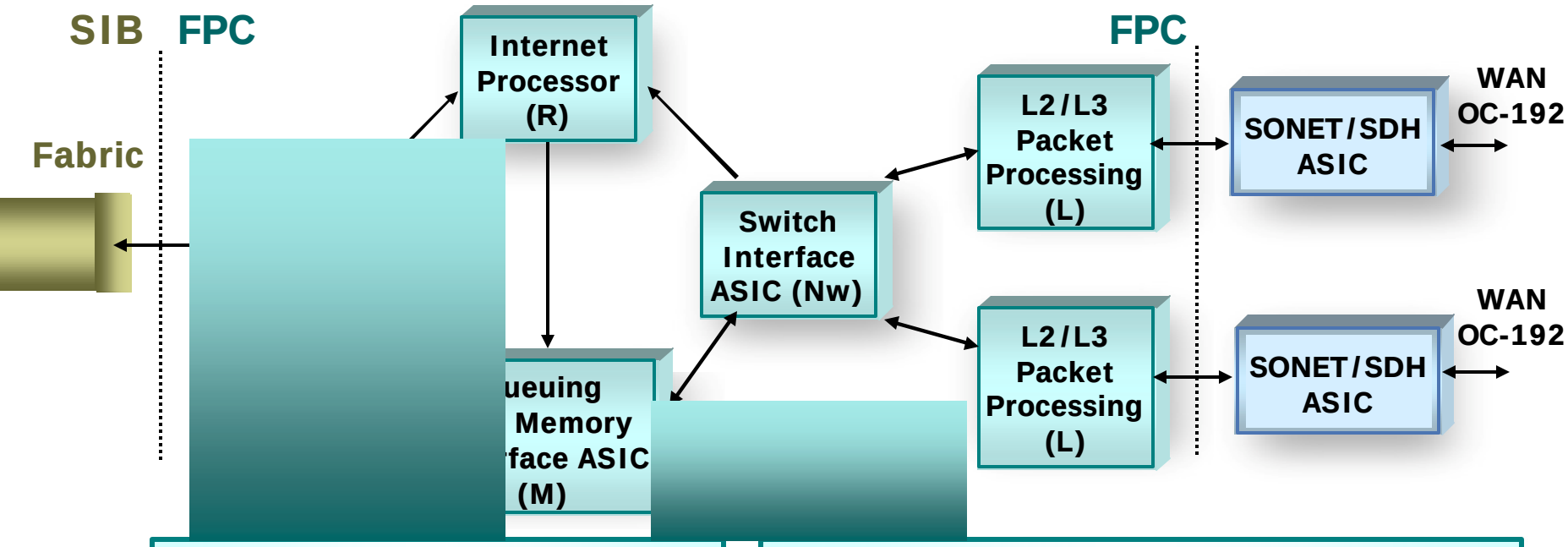
Egress Packet Flow



Re-sequence cells from fabric, extract lookup key, send data to memory (M), send key and data pointer to route lookup (R)

Store packet data in memory

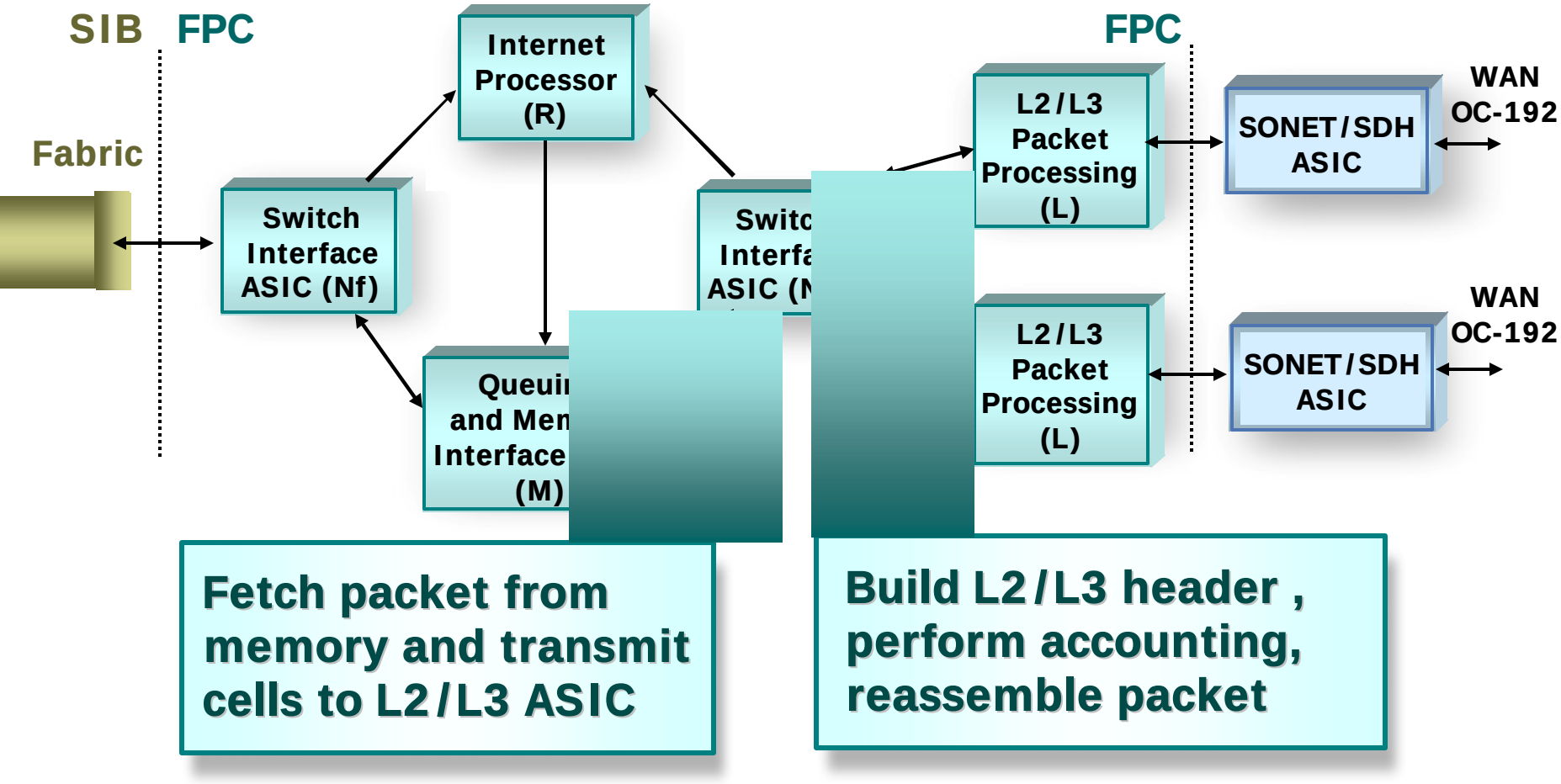
Egress Packet Flow



Perform route lookup, filtering, policing and queue selection

Queue packet pointers, perform WDRR scheduling, shape output bandwidth, RED drop

Egress Packet Flow



Agenda

Introduction

Packet Forwarding Engine

Routing Engine

Packet Flow Example

Summary

Summary

- JUNOS Platform Routers
  - Common ASIC technology
  - Common architecture
  - Common JUNOS software
  - Common Interfaces
- Clean separation of routing and packet forwarding functions
  - Consistent performance with flexibility
  - Built for stability and scalability

Thank You

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